Amendments To The Claims:

Claim 1 (currently amended): A system comprising:

a first processor including a first processor data channel;

a first hybrid switching module including a first hybrid switching module processor data channel, a first hybrid switching module main data channel, a first input/output link data channel, [[and]] a first ~~switch~~crossbar switch and arbiter, and a first bridge, the first hybrid switching module processor data channel being coupled to the first processor data channel;

a first main bus coupled to the first hybrid switching module main data channel;

a second processor including a second processor data channel; and

a second hybrid switching module including a second hybrid switching module processor data channel, a second input/output link data channel, [[and]] a second ~~switch~~crossbar switch and arbiter, and a second bridge, the second hybrid switching module processor data channel being coupled to the second processor data channel, the second input/output link data channel being coupled to the first input/output link data channel;

wherein the first hybrid switching module further comprises a failure mode that couples the first input/output link data channel with the first main bus when the first processor fails allowing the second processor to access the first main bus, and the second hybrid switching module further comprises a failure mode that couples the second input/output link data channel with the second main bus when the second processor fails allowing the first processor to access the second main bus.

Claim 2 (original): The system of Claim 1 wherein said second hybrid switching module further comprises a second hybrid switching module main data channel, wherein said system further comprises:

a second main bus coupled to the second hybrid switching module main data channel.

Claim 3 (original): The system of Claim 1 further comprising:

a third processor including a third processor data channel; and

a third hybrid switching module including a third hybrid switching module processor data channel, a third input/output link data channel, a fourth input/output link data channel, and a third switch, the third hybrid switching module processor data channel being coupled to the third processor data channel;

wherein said first hybrid switching module further comprises a fifth input/output link data channel;

wherein the third input/output link data channel is coupled to the fifth input/output link data channel;

wherein said second hybrid switching module further comprises a sixth input/output link data channel;

wherein the fourth input/output link data channel is coupled to the sixth input/output link data channel.

Claim 4 (original): The system of Claim 3 wherein said second hybrid switching module further comprises a second hybrid switching module main data channel, wherein said system further comprises:

a second main bus coupled to the second hybrid switching module main data channel.

Claim 5 (original): The system of Claim 4 wherein said third hybrid switching module further comprises a third hybrid switching module main data channel, wherein said system further comprises:

a third main bus coupled to the second hybrid switching module main data channel.

Claim 6 (currently amended): [[A]] An apparatus comprising:

a first hybrid switching module comprising:

a first hybrid switching module processor data channel;

a first hybrid switching module main data channel;

an input/output link data channel;

a first switch coupled to the first hybrid switching module processor data channel; and

a first bridge coupled to the first hybrid switching module main data channel;

wherein the first switch selectively couples to the first bridge and selectively couples to the input/output link data channel, wherein the first hybrid switching module processor data channel is thereby selectively coupled to the first bridge and selectively coupled to the input/output link data channel.

Claim 7 (currently amended): The apparatus of Claim 6 further comprising a first processor coupled to the first hybrid switching module processor data channel.

Claim 8 (currently amended): The apparatus of Claim 6 further comprising a first main bus coupled to the first bridge.

Claim 9 (currently amended): The apparatus of Claim 6 further comprising ~~another~~ a second switch coupled to the input/output link data channel.

Claim 10 (currently amended): The apparatus of Claim 9 further comprising ~~another~~ second bridge coupled to the ~~other~~ second switch.

Claim 11 (currently amended): The apparatus of Claim 10 further comprising:

a first main bus coupled to the first bridge; and

a second main bus coupled to the ~~other~~ second bridge.

Claim 12 (currently amended): The apparatus of Claim 9 further comprising:

a first processor coupled to the first hybrid switching module processor data channel; and

a second processor coupled to ~~another~~ a second hybrid switching module processor data channel, the ~~other~~ second switch being coupled to the ~~other~~ second hybrid switching module processor data channel.

Claim 13 (currently amended): A system comprising:

a first hybrid switching module processor data channel;

a first hybrid switching module main data channel;

a first hybrid switching module bus data channel;

an input/output link data channel; and

a first hybrid switching module coupled to the first hybrid switching module processor data channel and to the first hybrid switching module main data channel;

wherein the first hybrid switching module selectively couples to the [[a]] first hybrid switching module bus data channel and selectively couples to the input/output link data channel, wherein the first hybrid switching module processor data channel is thereby selectively coupled to the first hybrid switching module bus data channel and

selectively coupled to the input/output link data channel, and the first hybrid switching module further comprises a failure mode that couples the input/output link data channel with the first hybrid switching module bus data channel during a failure.

Claim 14 (currently amended): The apparatus of Claim 13 further comprising a first processor coupled to the first hybrid switching module processor data channel.

Claim 15 (currently amended): The apparatus of Claim 13 further comprising a first main bus coupled to the first hybrid switching module bus data channel.

Claim 16 (currently amended): The apparatus of Claim 13 further comprising ~~another~~ a second hybrid switching module coupled to the input/output link data channel.

Claim 17 (currently amended): The apparatus of Claim 16 further comprising:

a first main bus coupled to the first hybrid switching module; and

a second main bus coupled to the ~~other~~ second hybrid switching module.

Claim 18 (currently amended): The apparatus of Claim 16 further comprising:

a first processor coupled to the first hybrid switching module processor data channel; and

a second processor coupled to ~~another~~ a second hybrid switching module processor data channel, the ~~other~~ second hybrid switching module being coupled to the ~~other~~ second hybrid switching module processor data channel.